RF/Microwave Circuit Design for Wireless Applications. Ulrich L. Rohde, David P. Newkirk

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APPENDIX B

NONLINEAR MICROWAVE CIRCUIT DESIGN USING MULTIHARMONIC LOAD-PULL SIMULATION TECHNIQUE*

This appendix presents practical applications of the multiharmonic load-pull simulation technique to the design of nonlinear microwave circuits. A systematic scheme using multiharmonic load-pull simulation explores the effects of each harmonic termination on the circuit performance and finds the optimal load at each harmonic. The circuit performance can significantly be improved following this systematic design procedure. This approach provides an efficient means of nonlinear microwave circuit design. Its advantages are illustrated for the design of two power amplifiers and a frequency doubler.

B-1 INTRODUCTION

With the rapid development of wireless communication in recent years, the quality of the nonlinear circuits, such as power amplifiers, oscillators, and frequency doublers, is becoming an increasingly critical component of the entire communication system. A good design of such nonlinear circuits can significantly improve the performance of the system and reduce its cost.

The harmonic-balance (HB) technique has widely been used for nonlinear microwave circuit design since its implementation in commercial CAD software. Many new applications have been developed for the HB method such as stability analysis [1, 2] and load-pull simulation [3]. Load-pull techniques and harmonic load tuning have been used successfully for large-signal device characterization and nonlinear circuit design (e.g., [4–7]). However,

*This appendix is based on Qian Cai, Jason Gerber, Chao-Ren Chang, and Ulrich L. Rohde, "Nonlinear Microwave Circuit Design Using Multi-harmonic Load-Pull Simulation Technique," *Int. J. Microwave Millimeter-Wave Computer-Aided Eng.*, 1999.

the design procedure has never been described systematically. This prevents or restricts the practical usage of the load-pull techniques.

Here we present a systematic scheme to use the load-pull technique efficiently in nonlinear microwave circuit design. Multiharmonic load-pull simulation using the HB method is used as a vehicle for our presentation. Response contours are simulated by sampling the corresponding harmonic impedance of the selected tuner connected to the input or output port. Optimal harmonic impedances are located from the response contours. A step by step design procedure is described.

Our process can be classified into two major steps: finding the optimal loading at each harmonic and checking the power levels of higher harmonics. By checking the power levels of higher harmonics, we can readily see the effects of higher harmonic loading on the circuit performance. Further steps are carried out based on the investigation of the higher harmonic loading effects. It is a very effective way for microwave engineers to achieve good, if not the best, results in nonlinear circuit design.

The multiharmonic load-pull simulation is presented in Section B-2. Applications of multiharmonic load-pull simulation to nonlinear circuit design are addressed in Section B-3. The circuit designs of two power amplifiers and a frequency doubler are demonstrated.

B-2 MULTIHARMONIC LOAD-PULL SIMULATION USING HARMONIC BALANCE

B-2-1 Formulation of Multiharmonic Load-Pull Simulation

The multiharmonic load-pull simulation is implemented within the nonlinear simulator, Microwave Harmonica [8], which uses an efficient HB technique [9]. The circuit topology for the multiharmonic load-pull simulation can be sketched generally as Figure B-1, where M tuners are placed at the M external ports considered. The formulation can generally be expressed as

$$E(X, Z) = 0 \tag{B-1}$$

where E is the vector of HB errors, X is the set of all harmonic state variables, and Z is the set of harmonic loads on all external ports. The kth subvector of E can be written

$$E_k(X, Z) = A(k\omega_0, Z)\Phi(X, Z) + B(k\omega_0, Z)\Psi(X, Z) + D(k\omega_0, Z) \tag{B-2}$$

where $0 \le k \le N_H$ (N_H is the number of harmonics used in the simulation), A and B are circuit matrices, D is a set of driving functions, and Φ and Ψ are, respectively, the harmonic vectors of instantaneous voltages v and currents i at the nonlinear subnetwork ports.

The harmonic loads Z can be written in the following matrix form:

$$Z = \begin{bmatrix} Z_1(0\omega_0) & Z_1(1\omega_0) & \cdots & Z_1(N_H\omega_0) \\ Z_2(0\omega_0) & Z_2(1\omega_0) & \cdots & Z_2(N_H\omega_0) \\ \vdots & \vdots & \vdots & \vdots \\ Z_M(0\omega_0) & Z_M(1\omega_0) & \cdots & Z_M(N_H\omega_0) \end{bmatrix} \tag{B-3}$$

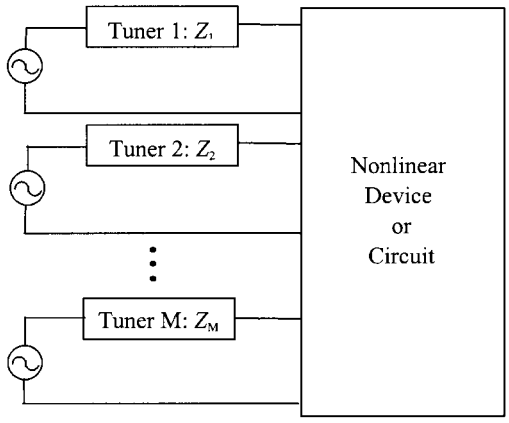


Figure B-1 Circuit topology for multiharmonic load-pull simulation.

where M is the number of external ports considered and $Z_i(k\omega_0)$ is the load at the kth harmonic and the ith port with $(0\omega_0)$ representing the dc component. The purpose of multiharmonic load-pull simulation is to find the optimal harmonic loading with respect to the design specifications. An impedance sampling method is used in our implementation of multiharmonic load-pull simulation. Only one component of Z is sampled at the defined impedance plane while the others are kept constant at each step. The HB simulation is performed at each sampling point to solve for the circuit responses specified. After the simulations are finished at all sampling points, load-pull contours are plotted on the Smith Chart and then the optimal point is located.

B-2-2 Systematic Design Procedure

Without losing generality, and for easy illustration, we consider the two-port circuit shown in Figure B-2, where tuners are placed at the source and load ports. The impedance sampling is achieved by adjusting the tuner parameters, which can be described as follows.

$R_i(k\omega_0)$—The resistance at the ith tuner and the kth harmonic, $i = 1, 2$, and $k = 1, 2, \ldots, N_H$.
$X_i(k\omega_0)$—The reactance at the ith tuner and the kth harmonic, $i = 1, 2$, and $k = 1, 2, \ldots, N_H$.

In order to obtain a uniform sampling of points, the tuner impedance is mapped to a reflection coefficient using a reference impedance Z_r and the mapping equation

$$\Gamma_i(k\omega_0) = \frac{Z_i(k\omega_0) - Z_r}{Z_i(k\omega_0) + Z_r} \tag{B-4}$$

The impedance sampling is transferred to two sweeps: the magnitude of $\Gamma_i(k\omega_0)$ $[|\Gamma_i(k\omega_0)|]$ from 0 to 1 and the angle of $\Gamma_i(k\omega_0)$ $[\angle\Gamma_i(k\omega_0)]$ from 0° to 360°. Only the impedance at one selected tuner i and one harmonic k, that is, $\Gamma_i(k\omega_0)$, is allowed to be tuned at a time and the other harmonic impedances are fixed at any meaningful values. In the following presentation we select $Z_r = 50\ \Omega$.

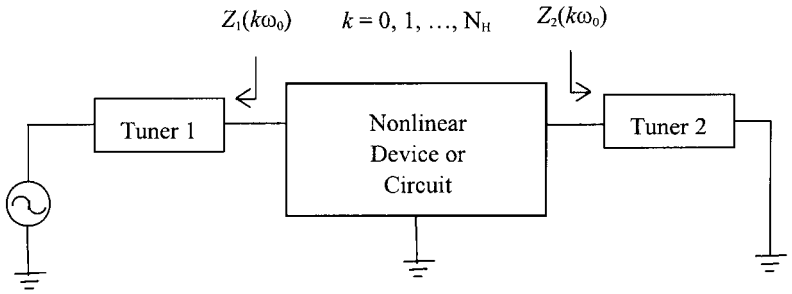


Figure B-2 Circuit schematic of a typical two-port nonlinear circuit.

The systematic design procedure can be described as follows:

Step 1: Start load-pull simulation by sampling the impedance at the fundamental frequency $Z_i(\omega_0)$ and find the optimal load $Z_{io}(\omega_0)$.

Step 2: Fix $Z_i(\omega_0)$ at $Z_{io}(\omega_0)$ and check the output spectrum to see the effects of higher harmonic loads on the circuit responses. If the effects of higher harmonic loads are significant, let $k = 2$, and go on to *Step 3*. Otherwise stop.

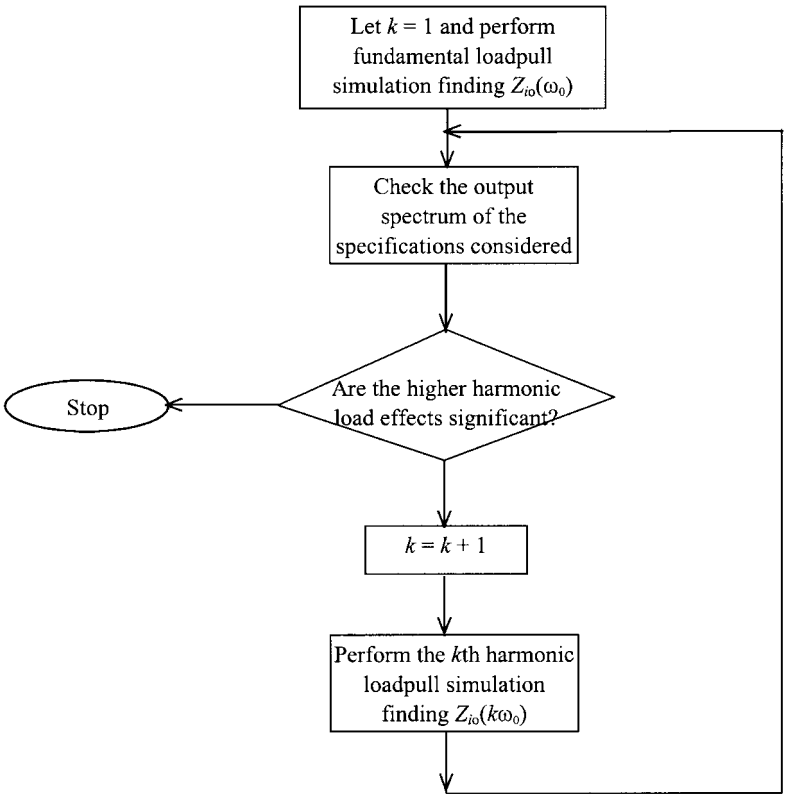


Figure B-3 Flowchart of design procedure using multiharmonic load-pull simulation.

Step 3: Perform load-pull simulation by sampling the kth harmonic impedance $Z_i(k\omega_0)$ and find the optimal load $Z_{io}(k\omega_0)$.

Step 4: Fix $Z_i(k\omega_0)$ at $Z_{io}(k\omega_0)$ and check the output spectrum to see the effects of higher harmonic loads on the circuit responses. If the effects of higher harmonic loads are significant, let $k = k + 1$, and go to *Step 3*. Otherwise stop.

This procedure can be repeated for all the tuners to achieve the optimal solution. It can be summed up as a load-pull simulation and spectrum-checking process. The flowchart in Figure B-3 illustrates this procedure.

B-3 APPLICATION OF MULTIHARMONIC LOAD-PULL SIMULATION

B-3-1 Narrowband Power Amplifier Design

Two power amplifiers, Amplifier 1 and Amplifier 2, are considered. The amplifiers are designed to operate at 0.5 GHz. The circuit schematic used for amplifier design is shown in Figure B-4. A Siemens power MESFET CLY10 [10] is used in our design. The MESFET is modeled by the modified Materka model [11] implemented in Microwave Harmonica [8]. Without losing generality, and for easy illustration, we fix all harmonic impedances of Tuner 1 (at the source port) at 50 Ω and tune Tuner 2 (at the load port) for both examples. Six harmonics are used in the HB simulation.

In Amplifier 1, the MESFET is biased at $V_{gs} = -1.3$ V and $V_{ds} = 5$ V, and the amplifier is designed as a normal Class A type with an input power of 10 dBm. Following the procedure described above, we perform load-pull simulation by sampling $Z_2(\omega_0)$ of Tuner 2 while other harmonic impedances of Tuner 2 are fixed at 50 Ω. The load-pull contours of power gain and power-added efficiency (PAE) are plotted in Figure B-5. The optimal load $Z_{2o}(\omega_0)$ is found to be $9.07 + j12.99$, at which the power gain is 18.54 dB and PAE is about 20%. The output power spectrum at this point is plotted in Figure B-6. By checking the output power spectrum of Figure B-6, we can see that the power levels at all higher harmonics are very small. Therefore, the higher harmonic loads will not have significant effects on the amplifier performance. To verify this conclusion, we perform load-pull simulation by sampling $Z_2(2\omega_0)$ of Tuner 2 while $Z_2(\omega_0)$ is fixed at $Z_{2o}(\omega_0)$. It is found that the best performance with respect to power gain and PAE is obtained for purely reactive second-harmonic loads, which is consistent with the results obtained by Berini et al. [5]. The output power versus the phase of $\Gamma_2(2\omega_0)$ is shown in Figure B-7, from which we can see that the influence of $Z_2(2\omega_0)$ is very small and our conclusion is justified.

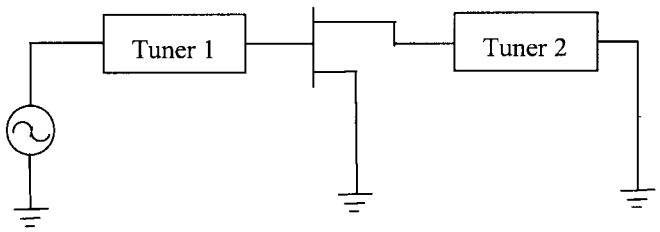
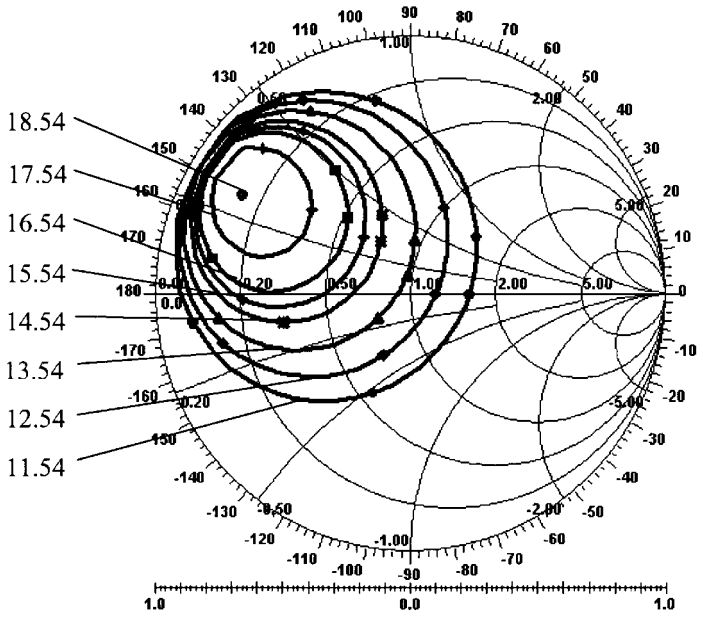
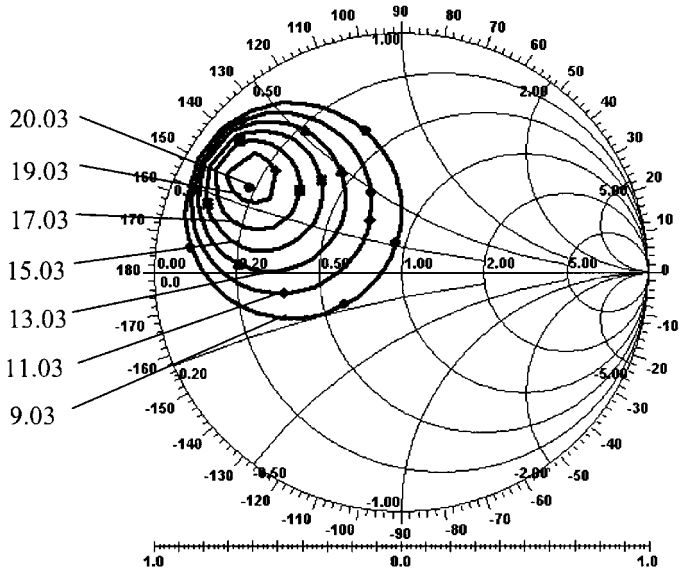


Figure B-4 Circuit topology for the amplifier design using multiharmonic load-pull simulation.



(a)



(b)

Figure B-5 Load-pull contours of (a) power gain (dB) and (b) PAE (%) of Amplifier 1 obtained from fundamental load-pull simulation.

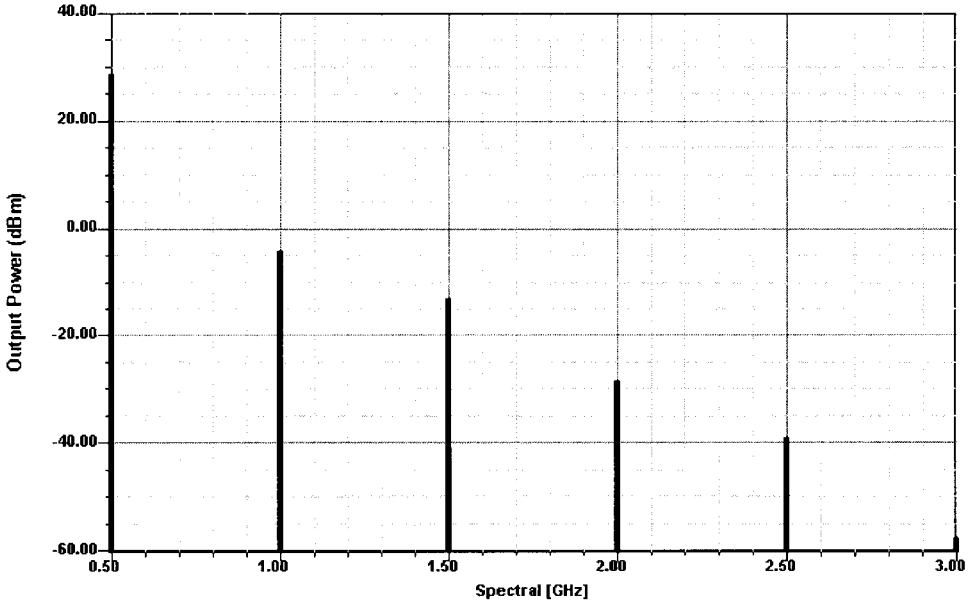


Figure B-6 Output power spectrum of Amplifier 1 when $Z_2(\omega_0) = Z_{2o}(\omega_0)$.

In order to illustrate the effects of higher harmonic loading on the amplifier performance, the MESFET is biased at $V_{gs} = -2.0$ V and $V_{ds} = 5$ V, and the input power is increased to 20 dBm in Amplifier 2. Figure B-8 shows the contours of power gain and PAE at the fundamental load-pull simulation. The optimal load $Z_{2o}(\omega_0)$ is $4.31 + j13.30$ for power gain (12.66 dB)

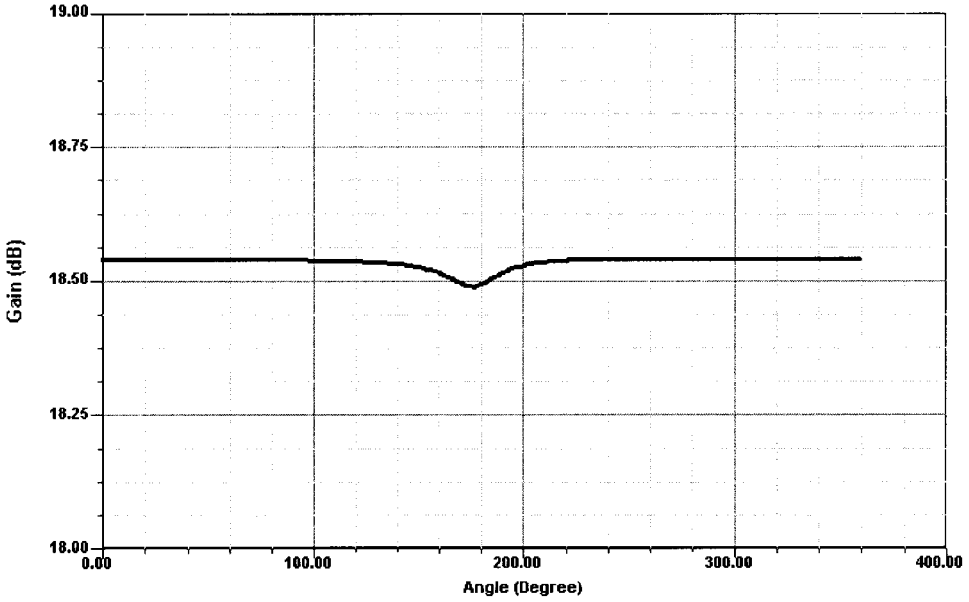
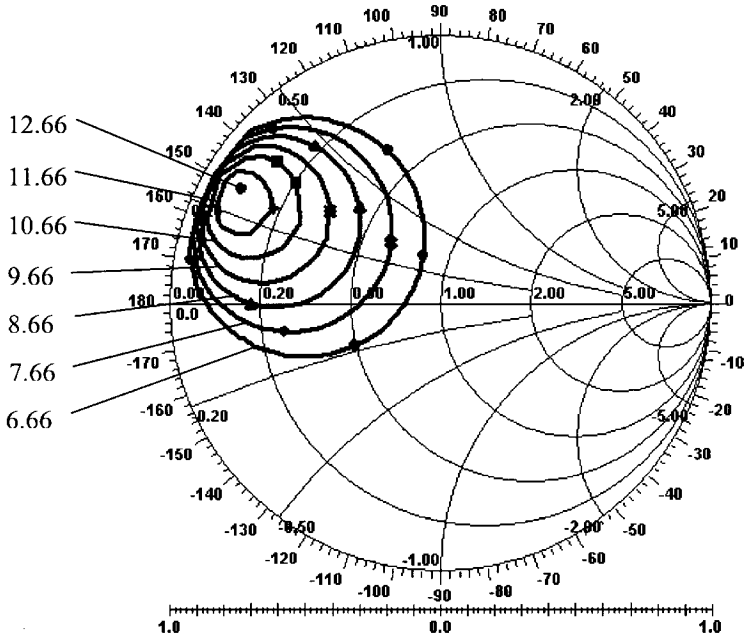
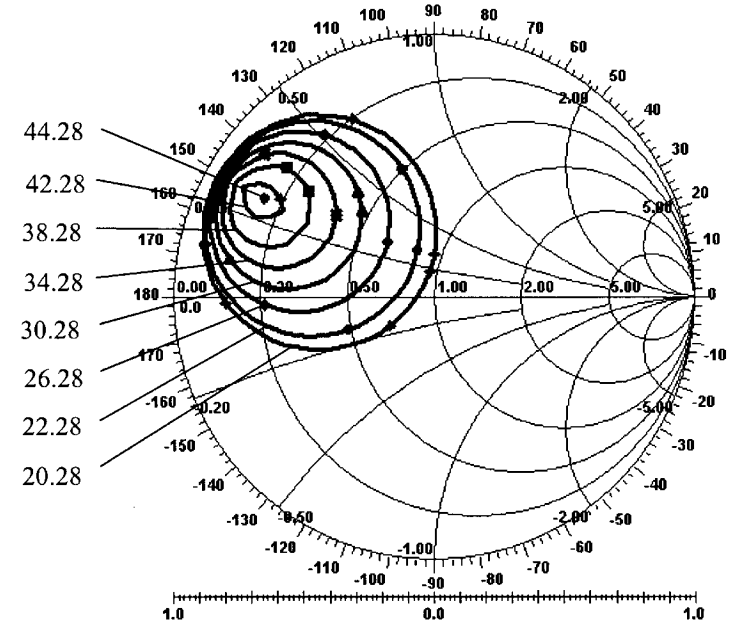


Figure B-7 Power gain versus the phase of $\Gamma_2(2\omega_0)$ for Amplifier 1.



(a)



(b)

Figure B-8 Load-pull contours of (a) power gain (dB) and (b) PAE (%) of Amplifier 2 obtained from fundamental load-pull simulation.

and 7.61 + j13.11 for PAE (44.28%). Though a compromise between the power gain and PAE can be obtained, we select 7.61 + j13.11 as our $Z_{2o}(\omega_0)$ and consider the PAE as the primary specification throughout the following process. The output spectrum at this point is shown in Figure B-9, which indicates that the output power levels at higher harmonics are significant, and thus the higher harmonic loads are critical to the amplifier performance.

By fixing $Z_2(\omega_0)$ at 7.61 + j13.11 and sampling $Z_2(2\omega_0)$, we perform the second-harmonic load-pull simulation. The contours of PAE are shown in Figure B-10, which also indicates that the best point for the second-harmonic load will be pure reactance near the short-circuit point. The effect of the phase of $\Gamma_2(2\omega_0)$ on PAE is shown in Figure B-11. The optimal value of $Z_{2o}(2\omega_0)$ is –j6.58, where the phase of $\Gamma_2(2\omega_0)$ is 195°. The PAE is improved from 44.28% to 47.18%. The output power spectrum at $Z_2(\omega_0)$ = 7.61 + j13.11 and at $Z_2(2\omega_0)$ = –j6.58 is shown in Figure B-12. From Figure B-12, we can see that the amplifier performance can be further improved by a proper third-harmonic load. The third-harmonic load-pull simulation is carried out by sampling $Z_2(3\omega_0)$ while $Z_2(\omega_0)$ and $Z_2(2\omega_0)$ are maintained at their optimal values. $Z_{2o}(3\omega_0)$ is found to be –j65.16 at which the value of PAE is 47.66%. Following the same procedure, we perform load-pull simulations up to the sixth harmonic. The results are as follows:

Harmonic Load	Optimal Value
$Z_2(\omega_0)$	7.61 + j13.11
$Z_2(2\omega_0)$	–j6.58
$Z_2(3\omega_0)$	–j65.16
$Z_2(4\omega_0)$	–j2.18
$Z_2(5\omega_0)$	–j28.81
$Z_2(6\omega_0)$	–j23.32

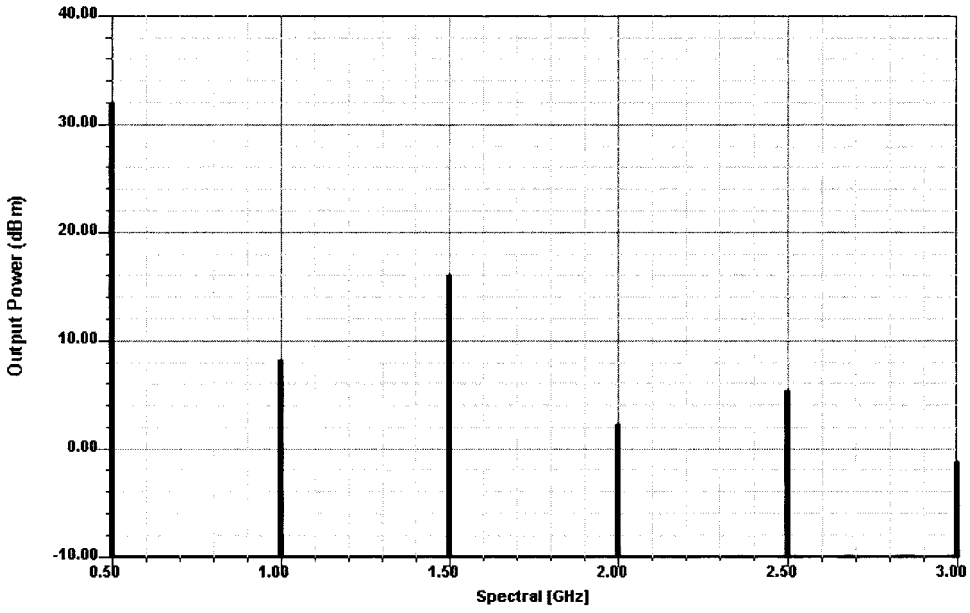


Figure B-9 Output power spectrum of Amplifier 2 when $Z_2(\omega_0) = Z_{2o}(\omega_0)$.

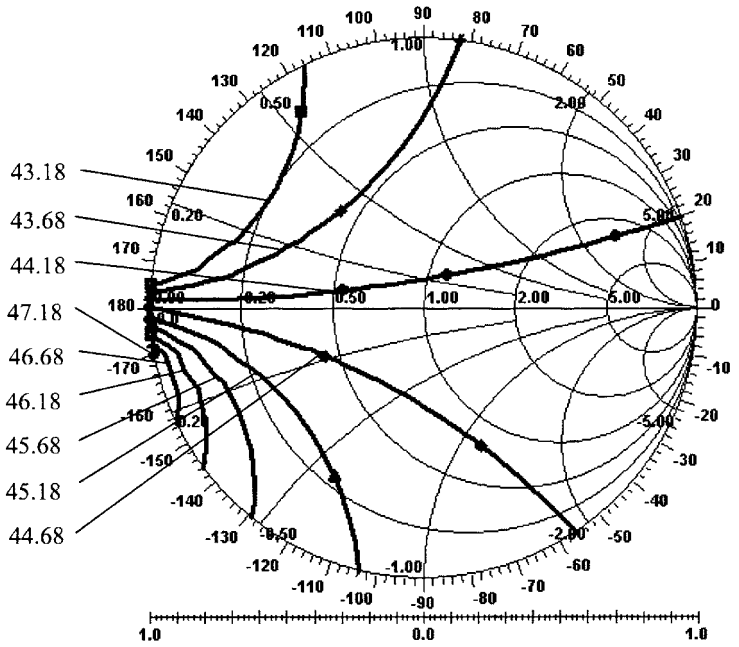


Figure B-10 Load-pull contours of PAE (%) of Amplifier 2 obtained from the second-harmonic load-pull simulation.

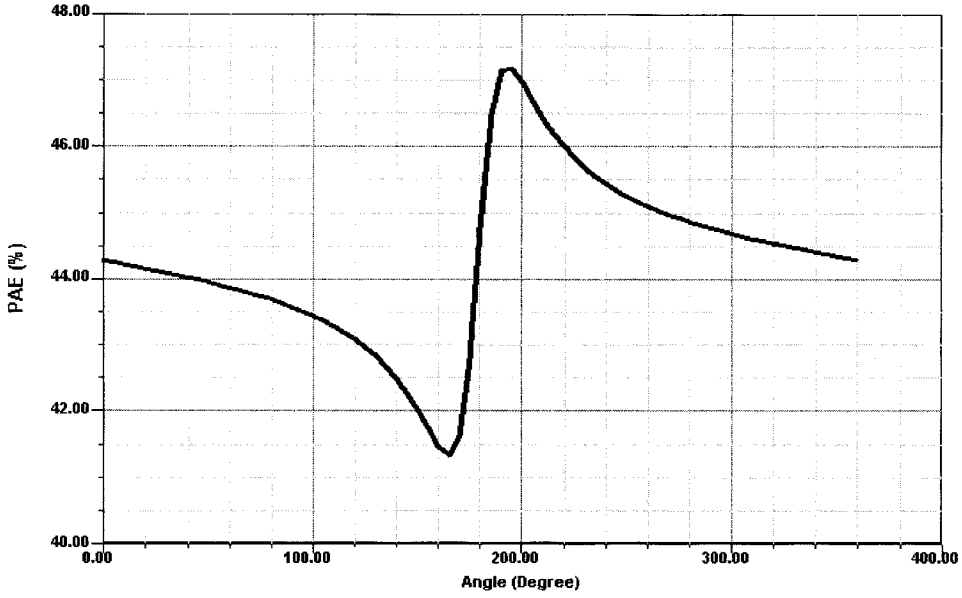


Figure B-11 PAE versus the phase of $\Gamma_2(2\omega_0)$ for Amplifier 2.

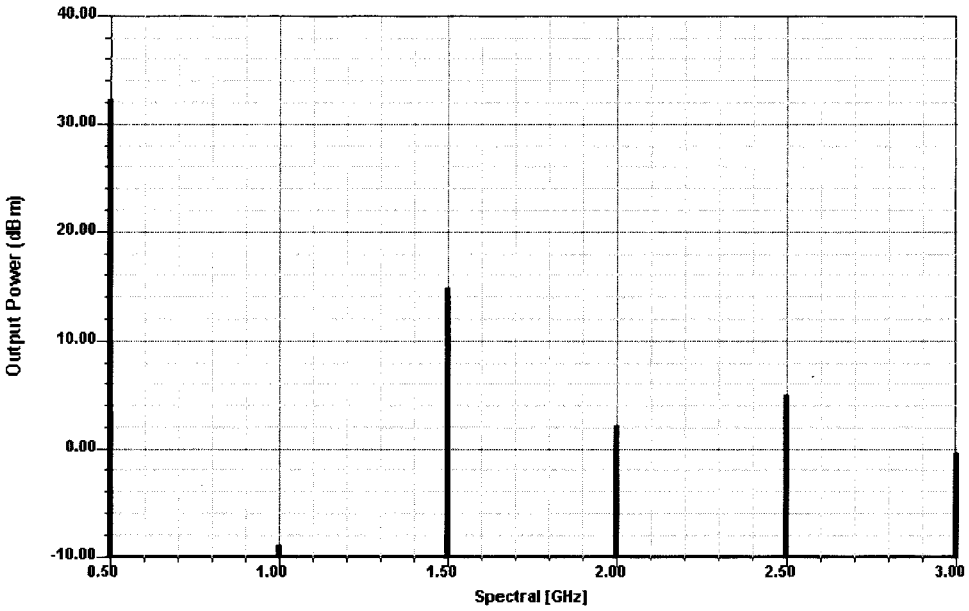


Figure B-12 Output power spectrum of Amplifier 2 when $Z_2(\omega_0) = Z_{2o}(\omega_0)$ and $Z_2(2\omega_0) = Z_{2o}(2\omega_0)$.

The PAE is 48.13% and power gain is 12.38 dB at the final design. The output power spectrum of the final design is shown in Figure B-13, which indicates that the output power levels at the second and higher harmonics have been suppressed significantly compared to the ones shown in Figure B-9.

B-3-2 Frequency Doubler Design

The circuit schematic shown in Figure B-14 is used for the frequency doubler design. The MESFET is biased at pinchoff, with $V_{gs} = -1.9$ V and $V_{ds} = 5$ V. The frequency of the input waveform is 5 GHz and the input power is 3 dBm. Six harmonics are considered in the HB simulation. Both Z_S and Z_L are 50 Ω. The conversion gain (CG) and the spectral purity (SP), are considered as the design specifications, calculated, respectively, by

$$CG = \frac{P_L(2\omega_0)}{P_{avs}(\omega_0)} \tag{B-5}$$

and

$$SP = \frac{P_L(2\omega_0)}{\sum_{k=1,\, k\neq 2}^{N_H} P_L(k\omega_0)} \tag{B-6}$$

where P_L is the power delivered to the load Z_L and P_{avs} is the available source power. In addition to the load-pull simulation, we also perform source-pull simulation in the design.

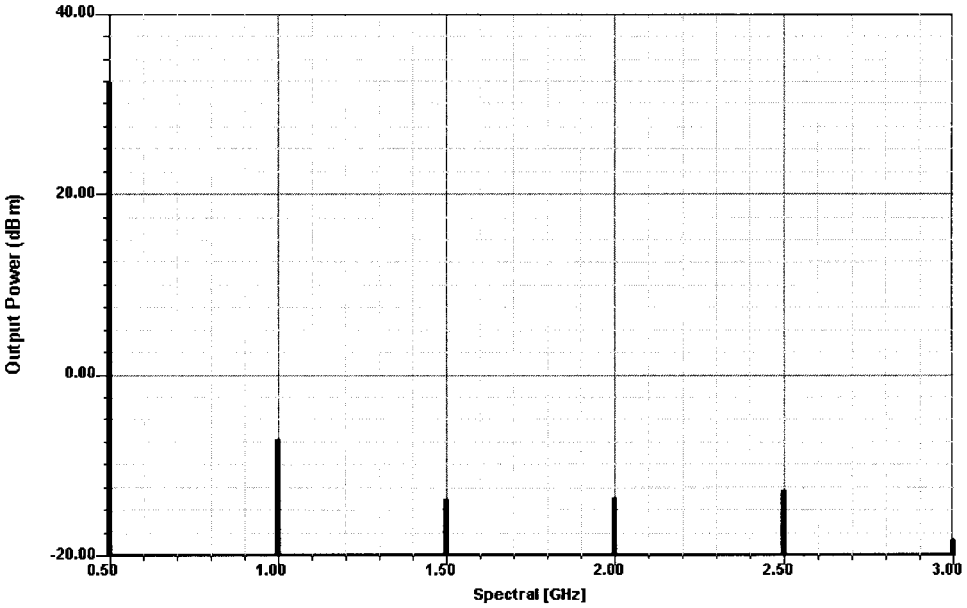


Figure B-13 Output power spectrum of Amplifier 2 at the final design.

Note that the harmonic impedance $Z_i(k\omega_0)$ is the tuner impedance without the load Z_L or the source impedance Z_S, and $\Gamma_i(k\omega_0)$ is the reflection coefficient of the tuner only in this design example.

First, the fundamental load-pull simulation is performed by sampling $\Gamma_2(\omega_0)$ at Tuner 2 while the impedances of all harmonics at Tuner 1 and other harmonic impedances of Tuner 2 are fixed at 0 Ω. The contours of SP with respect to $\Gamma_2(\omega_0)$ are plotted in Figure B-15, from which we can see that the optimal tuner impedance is infinity, which means that the fundamental harmonic component of the output waveform should be completely reflected by an open circuit. We select $1 \angle 0$ as the optimal point $[\Gamma_{2o}(\omega_0)]$, at which the SP is 13.21 dB and the CG is –9.75 dB. The second-harmonic load-pull simulation is performed by

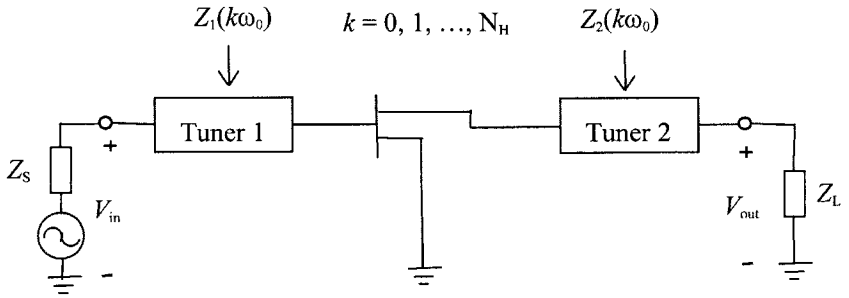


Figure B-14 Circuit topology for frequency doubler design using multiharmonic load-pull simulation.

sampling $\Gamma_2(2\omega_0)$ with $\Gamma_2(\omega_0)$ being fixed at $\Gamma_{2o}(\omega_0)$. The contours of SP with respect to $\Gamma_2(2\omega_0)$ are plotted in Figure B-16. The $\Gamma_{2o}(2\omega_0)$ is found to be $1 \angle 50$, at which the SP is improved from 13.21 to 18.14 dB and the CG from –9.75 to –5.89 dB. Following the same procedure, the load-pull simulation is performed up to the sixth harmonic. It is found that all the optimal harmonic impedances of Tuner 2 are infinity, except for the second harmonic, at which the optimal impedance is found to be $j127.23$. At the end of the load-pull simulation, the SP is 25.28 dB and the CG is –5.87 dB. The CG cannot be improved very much by tuning the harmonic impedances of Tuner 2.

The source-pull simulation is carried out by sampling the harmonic impedances of Tuner 1 using the same procedure as load-pull simulation with all the harmonic impedances of Tuner 2 being fixed at their optimal values. It is found that the most dominant harmonic impedance of Tuner 1 is the fundamental harmonic impedance. The optimal impedances at other harmonics of Tuner 1 turn out to be 0. The contours of CG with respect to $\Gamma_1(\omega_0)$ obtained by fundamental source-pull simulation with other harmonic impedances of Tuner 1 set to 0 Ω are plotted in Figure B-17. The $\Gamma_{1o}(\omega_0)$ is found to be $1 \angle 40$. The CG is significantly improved from –5.87 to 2.07 dB with a minor 0.5-dB degradation of spectral purity. The input and output voltage waveforms under the optimal termination conditions are shown in Figure B-18, from which we can see that the frequency of the output voltage is doubled to 10 GHz with a reasonable gain. The distortion of the input voltage waveform is due to the reflection of the higher-order harmonic voltages.

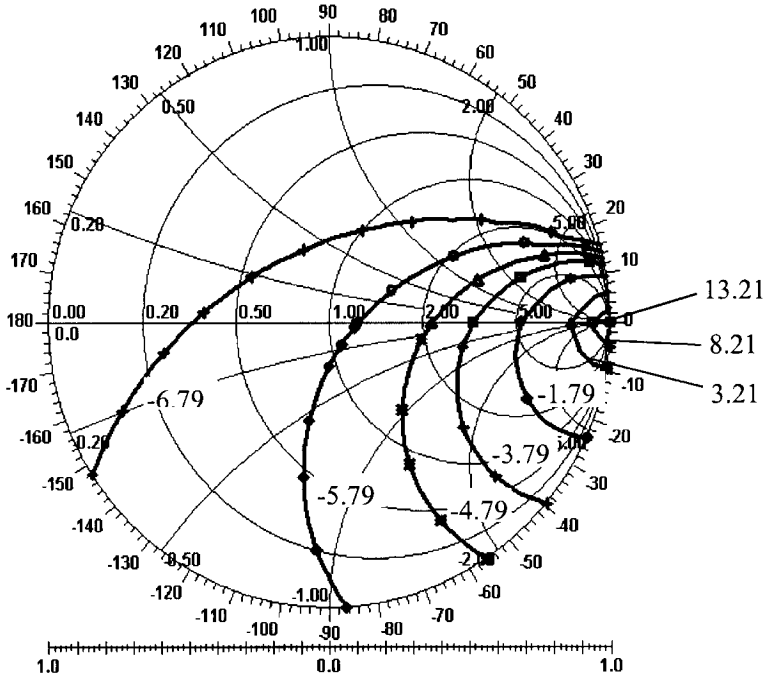


Figure B-15 Contours of spectral purity (dB) with respect to the fundamental impedance of Tuner 2 [$\Gamma_2(\omega_0)$] obtained from fundamental load-pull simulation of the frequency doubler.

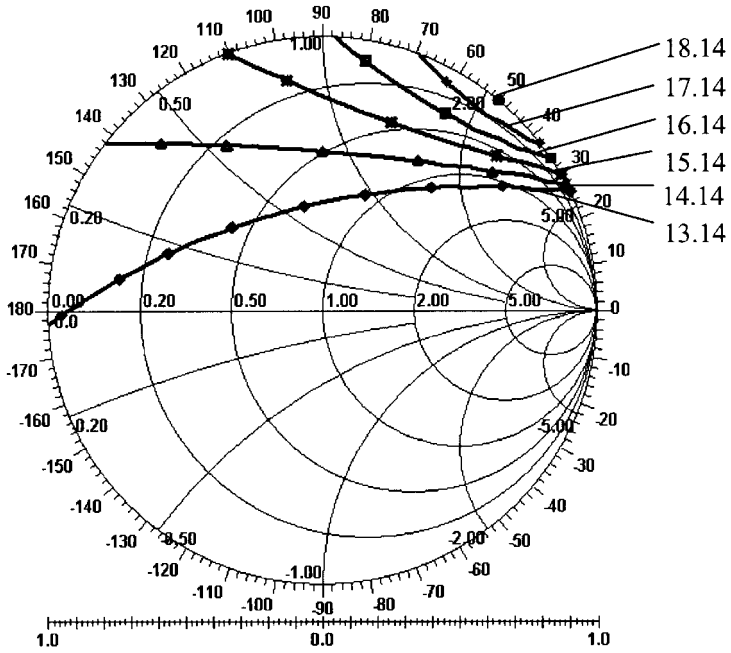


Figure B-16 Contours of spectral purity (dB) with respect to the second-harmonic impedance of Tuner 2 [$\Gamma_2(2\omega_0)$) obtained from the second-harmonic load-pull simulation of the frequency doubler.

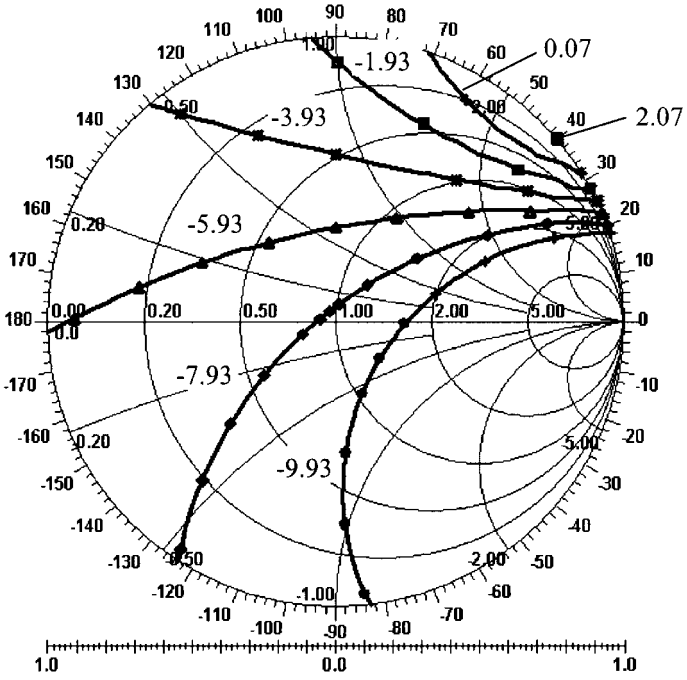


Figure B-17 Contours of conversion gain (dB) with respect to the fundamental impedance of Tuner 1 [$\Gamma_1(\omega 0)$] obtained from fundamental source-pull simulation of the frequency doubler.

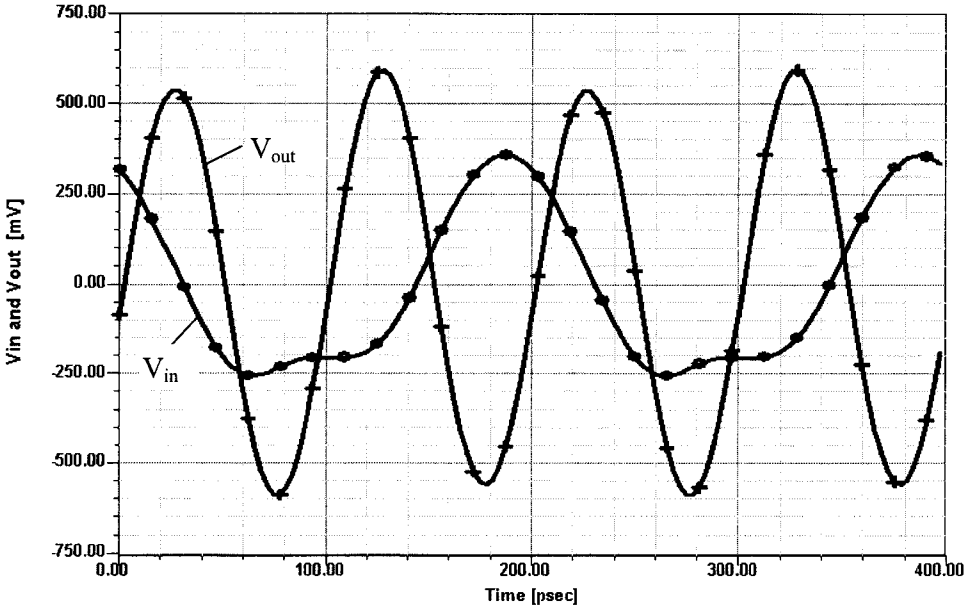


Figure B-18 Input and output voltage waveforms of the frequency doubler under the optimal termination conditions.

B-4 CONCLUSIONS

We have presented practical applications of multiharmonic load-pull simulation to the design of nonlinear microwave circuits. A systematic procedure has been addressed for effective circuit design. It has been demonstrated that the circuit performance can be improved significantly by a proper design of harmonic loads. This method can be applied to the design of nonlinear microwave circuits such as the power amplifier and frequency doubler to achieve the optimal solution and to utilize the maximum potential of the devices employed in the circuits.

B-5 NOTE ON THE PRACTICALITY OF LOAD-PULL-BASED DESIGN

From the standpoint that the wireless designer cannot have access to too many design aids, load-pull-based design techniques can serve as a valuable addition to the wireless designer's toolbox. We caution, however, that the current surge of interest in load-pull design techniques may owe as much to fashion and wishful thinking as it does to the practical achievability of the improved hardware performance that load-pull analysis may predict. Realizing the gain, PAE, and spectral-purity predictions of analyses like those presented here depends on the realization of optimum, controllable terminations at the signal fundamental *and its significant harmonics*—a nontrivial design challenge to say the least.

ACKNOWLEDGMENT

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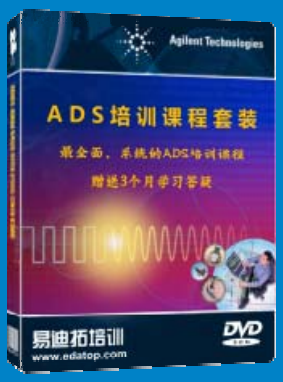

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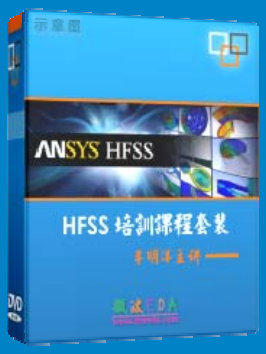

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